Remarks

Reconsideration of the rejections set forth in the Office Action dated May 1, 2006 is respectfully requested. Claims 1-6, 8-11, 19-27, and 37-46 have been rejected. Claim 47 has been added. As such, claims 1-6, 8-11, 19-27, and 37-47 are currently pending.

Claims 37 and 38 have been amended to remove the term "substantially," in a sincere effort to overcome the Examiner's rejections.

New claim 47 specifies that a circuit characteristic is a load characteristic. Support for this new claim may be found in the Specification, *e.g.*, on page 17.

Rejections under 35 U.S.C § 112

Claims 37 and 38 have been rejected under 35 U.S.C § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. The Examiner has indicated that he believes that the phrase "substantially" renders claims 37 and 38 as being indefinite. Claims 37 and 38 have been amended to remove the phrase "substantially."

In view of the amendments made to claims 37 and 38, it is respectfully submitted that the rejections of claims 37 and 38 under 35 U.S.C § 112, second paragraph, have been overcome.

Rejections under 35 U.S.C § 102 and 35 U.S.C § 103

Claims 1-3, 5, 8-11, 19, 21-24, 26, 27, 37, 38, and 44-46 have been rejected under 35 U.S.C § 102(e) as being anticipated by U.S. Patent Application Publication No. US 2002/0112072 of Jain (hereinafter "Jain"). Claims 4, 6, 20, 25, and 39-43 have been rejected

under 35 U.S.C § 103(a) as being unpatentable over Jain as applied to claims 1, 5, 12, 17, 19, and 24, and further in view of Applicant's admitted Prior Art.

1. Independent Claim 1, 19, 24 and their respective dependents

Independent claim 1 requires that a device includes a route generator and a list mechanism. The route generator is arranged to generate an alternate circuit path between a first node and a second node using a list mechanism stored on a memory. The list mechanism identifies a first element included in a primary circuit path. The route generator is arranged to accept an input that is arranged to specify one of a nodal diverse constraint and a link diverse constraint for the alternate circuit path. The input is also arranged to specify circuit characteristics for the primary circuit path and for the alternate circuit path. The alternate circuit path is generated so as not to include the first element identified by the list mechanism, and is not affected by a failure of the first element.

List Mechanism

Jain does not appear to disclose a list mechanism that is stored in memory. The Examiner has cited paragraphs [0078] and [0081] of Jain as teaching of a list mechanism that is stored in memory. It is respectfully submitted that paragraph [0078] discloses that label switched paths (LSPs) may be defined as alternate routes, and paragraph [0081] discloses that an LSP does not pass through an intermediate node. At best, these paragraphs disclose that alternate routes may be generated. However, there is no teaching or suggestion in these paragraphs that a list mechanism identifies a first element that is included in a primary circuit path, or that a list mechanism is stored in memory. Further, Jain does not appear to teach that a route generator uses the list mechanism to generate an alternate circuit path that does not include the first element.

The Applicants are unable to locate any teaching in Jain of any list mechanism stored in memory that identifies a first element which is not to be included in an alternate path, As such, claim 1 is believed to be allowable over the cited art for at least this reason.

Input arranged to specify Circuit Characteristics

The rejection of claim 1 is set forth on pages 3 and 4 of the Office Action dated May 1, 2006. It is noted that claim 1 recites "the input further being arranged to specify circuit characteristics for the primary circuit path and for the alternate circuit path." The Examiner appears not to have addressed this feature of claim 1 in his rejection of claim 1. However, the Applicants submit that Jain does not appear to teach of an input that specifies circuit characteristics for the primary circuit path and for the alternate circuit path. Accordingly, claim 1 is believed to be allowable over Jain for at least this reason as well.

It is noted that at paragraph [0102], Jain discloses that a recovery time criteria may be specified. A recovery time criteria appears to be a maximum amount of time necessary to restore traffic carried by a protected resource. The Applicants submit that the amount of time necessary to restore traffic carried by a protected resource does not anticipate circuit characteristics for a primary circuit path and for an alternate circuit path.

Claims 2-6, 8-11, 37, 38, and 46 each depend either directly or indirectly from claim 1, and are therefore each believed to be allowable over the cited art for at least the reasons set forth with respect to claim 1. Each of these claims recites additional limitations which, when considered in light of claim 1, are believed to further distinguish the claimed invention over the cited art.

Independent claims 19 and 24 recite similar limitations as recited in claim 1. Hence, claims 19, 24, and their respective dependents are each believed to be allowable over the cited art for at least the reasons set forth above with respect to claim 1.

2. Independent Claim 39 and its dependents

Independent claim 39 recites a device for computing circuit paths between a first node and a second node in a network that includes at least one protected element. The device includes a memory, a route generator, and a list mechanism. The route generator generates a primary circuit path including a first plurality of elements, and is arranged to accept an input that specifies a nodal diverse constraint or a link diverse constraint for an alternate circuit path. The input is also arranged to specify a load characteristic that is to be accounted for when the alternate circuit path is generated. The list mechanism identifies the first plurality of elements and the protected element, and the route generator generates the alternate circuit path using the list mechanism and the input such that the alternate circuit path does not include the first plurality of elements or the protected element.

The Examiner has argued that Jain in view of and the Applicants admitted Prior Art (AAPA) teach the invention of claim 39. The Applicant respectfully disagrees. As discussed above with respect to claim 1, Jain does not disclose a list mechanism that is stored in memory, or a route generator that uses the list mechanism to generate an alternate circuit path. Further, Jain does not appear to teach of a list mechanism that identifies a plurality of elements and at least one protected element. As AAPA also does not teach of or reasonably suggest the list mechanism, of claim 39, claim 39 is believed to be allowable over the cited art for at least the reasons set forth.

Claim 39 also recites that an input specifies a load characteristic that is to be accounted for when an alternate circuit path is generated. The Examiner has argued that paragraph [0102] of Jain teaches of an input that specifies a load characteristic. At best, paragraph [0102] of Jain appears to disclose that a recovery time criteria that is a maximum amount of time to restore traffic may be specified. The amount of time to restore traffic is not equivalent to, and does not anticipate, a load characteristic. Jain does not reasonably suggest specifying a load characteristic. Therefore, claim 39 is believed to be allowable over the cited art for at least this reason as well.

Claims 40-43 each depend from claim 39 and are, therefore, each believed to be allowable over the cited art for at least the reasons set forth above with respect to claim 39. Each of these dependent claims recites additional limitations which, when considered in light of claim 39, are believed to further distinguish the claimed invention over the art of record.

3. Independent Claim 44 and its dependent

Independent claim 44 recites a method for computing circuit paths between a first node and a second node in a network that includes a plurality of elements. The method involves receiving an input that is arranged to specify one of a nodal diverse constraint and a link diverse constraint, and circuit characteristics for a primary and alternate circuit path. The primary circuit path is generated, and the specified circuit characteristics are accounted for in the generation. A list that identifies a first element in the primary circuit path is created and stored in memory. The alternate circuit path is generated to not include the first element and to account for the specified circuit characteristics. In generating the alternate circuit path, the stored list is accessed, and the first element is identified as being blocked from use in routing the alternate circuit path.

It is respectfully submitted that Jain does not disclose creating a list that identifies a first element or storing the list in memory. The Examiner cites paragraphs [0080] and [0063] of Jain as disclosing these limitations. Paragraph [0080] of Jain appears to disclose that node may be identified, but does not disclose or suggest that a list that identifies a first element such as a node may be created and stored. Paragraph [0063] of Jain discloses that a shared resource link group (SRLG) that relates to possible points of failure may be stored. A SRLG is not a first element in a primary circuit path that is identified as being blocked from use in routing an alternate circuit path. As such, claim 44 is believed to be allowable over the cited art for at least this reason.

Claim 45 depends from claim 44 and is, therefore, believed to be allowable over the cited art for at least the reasons set forth above with respect to claim 44. Claim 45 also recites additional limitations which, when considered in light of claim 44, are believed to further distinguish claim 45 over the cited art. Claim 45 recites that specified circuit characteristics

include either a shortest path characteristic or a load balancing characteristic. While Jain mentions at paragraph [0084] that LSPs may be advantageous for load balancing, Jain does not appear to teach of a circuit characteristic that is specified in an input as providing for load balancing. Jain also does not appear to teach that a shortest path characteristic is specified as an input. Hence, claim 45 is believed to be allowable over the cited art for at least this additional reason as well.

Conclusion

For at least the foregoing reasons, the Applicants believe all claims now pending in this application are in condition for allowance and should be passed to issue. If the Examiner believes a telephone conference would in any way expedite prosecution of the application, please do not hesitate to contact the undersigned at (408)868-4096.

Respectfully submitted,

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